RECEIVED
CENTRAL FAX CENTER
AUG 2 2 2005

PATENT **AF01169**

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence (along with any paper referred to as being attached or enclosed) is being faxed to 571-273-8300 on the date shown below to Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Date: 8-22-05

Himanshu S. Amin

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Applicant(s): Ming-Huei Shieh, *et al.*

Serial No: 10/600,065

Filing Date: June 20, 2003

Examiner: Dang T. Nguyen

Art Unit: 2824

Title: MEMORY WITH A CORE-BASED VIRTUAL GROUND AND DYNAMIC REFERENCE SENSING SCHEME

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

08/23/2005 MBINAS 00000015 10600065
01 FC:1402 500.00 OP

APPEAL BRIEF

Dear Sir:

Applicant's representative submits this brief in connection with an appeal of the above-identified patent application. A credit card payment form is filed concurrently herewith in connection with all fees due regarding this appeal brief. In the event any additional fees may be due and/or are not covered by the credit card, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1063 [AMDP975US].

I. Real Party in Interest (37 C.F.R. §41.37(c)(1)(i))

The real party in interest in the present appeal is AMD Investments, Inc., the assignee of the present application.

II. Related Appeals and Interferences (37 C.F.R. §41.37(c)(1)(ii))

Appellant, appellant's legal representative, and/or the assignee of the present application are not aware of any appeals or interferences which may be related to, will directly affect, or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. Status of Claims (37 C.F.R. §41.37(c)(1)(iii))

Claims 1-27 are pending in the application. Claims 1-27 stand rejected by the Examiner. The rejections of claims 1-27 are being appealed.

IV. Status of Amendments (37 C.F.R. §41.37(c)(1)(iv))

No claim amendments have been entered after the Final Office Action.

V. Summary of Claimed Subject Matter (37 C.F.R. §41.37(c)(1)(v))

A. Independent Claim 1

Independent claim 1 recites an architecture that facilitates a reference voltage in a multi-bit memory, comprising a multi-bit memory core including a plurality of data cells for storing data; first and second reference arrays of a plurality of multi-bit reference cells, the first and second reference arrays fabricated on the memory core; and a first bit value of a first reference cell of the first reference array averaged with a second bit value of a second reference cell of the second reference array to arrive at the reference voltage employed during a data cell read operation. (*See, e.g.*: page 5, lines 2-8, lines 15-19, and lines 22-28; page 10, lines 9-22, page 11, lines 22-30; page 12, lines 3-12, lines 18-24; page 16, lines 3-33 to page 17, lines 1-4; *see also, generally,* Figures 1-9 and 11-14).

B. Independent Claim 13

Independent claim 13 recites An architecture that facilitates a reference voltage in a multi-bit memory, comprising a multi-bit memory core for storing data, the memory core including two groups of data sectors; first and second reference arrays of a plurality of multi-bit reference cells , the first and second reference arrays fabricated on the memory core interstitial to the groups of data sectors; and a first bit value of a first reference cell of the first reference array and a second bit value of a second reference cell of the second reference array forming a reference pair whose respective bit values are averaged to arrive at the reference voltage for a read operation. (*See, e.g.*: page 5, lines 2-8, lines 15-19, and lines 22-28; page 10, lines 9-22, page 11, lines 22-30; page 12, lines 3-12, lines 18-24; page 16, lines 3-33 to page 17, lines 1-4; *see also, generally,* Figures 1-9 and 11-14).

C. Independent Claim 17

Independent claim 17 recites a method for providing a reference voltage in a multi-bit memory, comprising receiving a multi-bit memory core for storing data; providing first and second reference arrays of a plurality of multi-bit reference cells, the first and second reference arrays fabricated on the memory core; and averaging a first bit value of a first reference cell of the first reference array with a second bit value of a second reference cell of the second reference array to arrive at the reference voltage utilized during a read operation. (*See, e.g.*: page 17, lines 14-33 to page 18, lines 1-24; *see also, generally,* Figure 11).

D. Independent Claim 24

Independent claim 24 recites a system for providing a reference voltage in a multi-bit memory, comprising means for providing a multi-bit memory core for storing data (*See, e.g.*: page 1, lines 7-9; page 5, lines 1-5 and lines 23-25; page 15, lines 17-19 to page 16, lines 1-2; page 17, lines 14-16 and lines 23-28; page 18, lines 26-29; *see also, generally,* Figures 1-14); means for providing first and second reference arrays of a plurality of multi-bit reference cells, the first and second reference arrays fabricated on the memory core (*See, e.g.*: page 5, lines 14-28; page 10, lines 23-30; page 11, lines 33 to page 12, lines 1-12; page 12, lines 15-28; page 16, lines 3-11 and lines 27-31; page 17, lines 21-26; page 18, lines 30-33 to page 19, lines 1-9; page 20, lines 13-15; page 21, lines 1-5; *see also, generally,* Figures 1-14); and means for averaging a first bit value of a first reference cell of the first reference array with a second bit value of a second reference cell of the second reference array to arrive at the reference voltage to facilitate a read operation. (*See, e.g.*: page 5, lines 1-5, lines 19-21, and lines 25-28; page 11, lines 24-33 page 12, lines 1-12; page 12, lines 20-28; page 13, lines 5-17; page 16, lines 27-33 to page 17, lines 1-4; page 18, lines 10-14, 17-24, and lines 20-33; page 19, lines 1-9 and lines 12-16; *see also, generally,* Figures 1-14).

VI. Grounds of Rejection to Be Reviewed (37 C.F.R. §41.37(c)(1)(vi))

A. Claims 1-15 and 17-26 stand rejected under 35 U.S.C. §102(e) as being anticipated by Le *et al.* (U.S. 6,690,602 B1).

B. Claims 13, 16, 24 and 27 stand rejected under 35 U.S.C. §102(e) as being anticipated by Kurihara *et al.* (U.S. 6,791,880 B1).

VII. Argument (37 C.F.R. §41.37(c)(1)(vii))

A. Rejection of Claims 1-15 and 17-26 Under 35 U.S.C. §102(e)

Claims 1-15 and 17-26 stand rejected under 35 U.S.C. §102(e) as being anticipated by Le *et al.* (U.S. 6,690,602 B1). It is respectfully requested that this rejection be withdrawn for at least the following reason. Le *et al.* does not teach or

suggest each and every limitation recited in the subject claims.

> A claim is anticipated only if ***each and every element*** as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ...claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Specifically, independent claim 1 recites "a first bit value of a first reference cell of the first reference array averaged with a second bit value of a second reference cell of the second reference array to arrive at the reference voltage employed ***during a data cell read operation***." Similarly, independent claims 13, 17, and 24 relate to the data cell read operation. During a data cell read operation, the first reference cell voltage and the second reference cell voltage can be averaged in order to determine whether a data bit is programmed or unprogrammed. (*See* Application, pg. 12, lines 9-10; and pg. 12, lines 23-24). Moreover, this determination is utilized during ***a data cell read operation***. (*See* Application, pg. 12, lines 3-7; and pg. 12, lines 18-21). Le *et al.* merely utilizes an averaging of voltage levels for <u>programming</u> within the memory cells. Yet, Le *et al.* does not teach or suggest utilizing such average voltage to be utilized during ***a data cell read operation*** as recited in the subject claims. Rather, Fig. 4 of Le *et al.* is a comparison circuit that can be utilized to compare the value ***read from a core cell*** to the averaged data read from the reference array. A read from a core cell is not a data cell read operation because the core contains a plurality of cells with respective values associated therewith. For example, a read of the data cell relates to the voltage level associated to the particular cell, whereas the read of a core pertains to the cumulative bitlines and wordlines within the core. Hence, while the cited reference is directed towards a *method of programming cells* in reference arrays (*See* Le *et al.*, col. 6, lines 17-19), it is silent towards arriving at a reference voltage ***utilized during a read operation*** as in the claimed invention.

In addition, the Examiner is reminded that the standard by which anticipation is to be measured is ***strict identity*** between the cited document and the invention as claimed,

not mere equivalence or similarity. *See*, *Richardson* at 9 USPQ2d 1913, 1920. This means that in order to establish anticipation under 35 U.S.C. §102, the single document cited must not only expressly or inherently describe each and every limitation set forth in the patent claim, but also the identical invention must be shown in as complete detail as is contained in the claim. The fact that Le *et al.* fails to provide utilizing a reference voltage during a data cell read operation leads one to believe that the cited document in the final analysis does not provide an invention identical to that recited in the subject claims.

In view of at least the foregoing comments, it is readily apparent that Le *et al.* does not teach or suggest each and every limitation of the independent claims 1, 13, 17, 24 (and claims 2-12, 14-16, 18-23, and 25-27 which respectively depend there from). Applicants' representative respectfully requests the withdrawal of this rejection.

B. Rejection of Claims 13, 16, 24 and 27 Under 35 U.S.C. §102(e)

Claims 13, 16, 24 and 27 stand rejected under 35 U.S.C. §102(e) as being anticipated by Kurihara *et al.* (U.S. 6,791,880 B1). It is respectfully requested that this rejection be withdrawn for at least the following reason. Kurihara *et al.* does not teach or suggest each and every limitation recited in the subject claims.

In particular, independent claims 13 and 24 implement an average of ***a first bit value of a first reference cell and a second bit value of a second reference cell*** to arrive at a reference voltage for a read operation. Kurihara *et al.* does not teach or suggest an average of a first bit value of a first reference cell and a second bit value of a second reference cell, but rather simulates beginning of life (BOL) behavior of memory cell. Specifically, Kurihara *et al.* utilizes an adjustable current source (460) with a selected column of a memory cell (455) and a disparate adjustable current source (485) for a disparate memory cell (480) as inputs to cascode 445 and cascode 470 respectively. (*See* Fig. 4). The adjustable current source provides end of life (EOL) simulation for the reference current source, so that the beginning of life (BOL) behavior of the sense amplifier and its inputs can be evaluated. (*See* col. 4, lines 55-60). The ***cascode 445 and cascode 470 can provide a combined output that is an average of their inputs*** when switches 440 and 465 are closed. (*See* col. 5, lines 20-24, emphasis added). The input to cascode 445 is the current associated with the column (*e.g.*, wordline determined by the

Y decoder 450) in the memory cell 455 and the current from the adjustable current source 460. Similarly, the input to cascode 470 is the current associated with the column (determined by the Y decoder 475) in the memory cell 480 and the current from the adjustable current source 485. (*See* Fig. 4). Thus, with the input to the cascode 445 and 470 being a current and an adjustable current source, the average provided contains the current from two memory cells plus the current from two adjustable sources.

In view of at least the foregoing, it is readily apparent that Karihara *et al.* does not teach or suggest each and every limitation of independent claims 13 and 24 (and claims 16 and 27 which respectively depend there from). Applicants' representative respectfully requests the rejection be withdrawn.

C. Conclusion

For at least the above reasons, the claims currently under consideration are believed to be patentable over the cited references. Accordingly, it is respectfully requested that the rejections of claims 58-75 be reversed.

If any additional fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063.

Respectfully submitted,
AMIN & TUROCY, LLP

Himanshu S. Amin
Reg. No. 40,894

AMIN & TUROCY, LLP
24th Floor, National City Center
1900 East 9th Street
Telephone: (216) 696-8730
Facsimile: (216) 696-8731

VIII. Claims Appendix (37 C.F.R. §41.37(c)(1)(viii))

1. (Previously Presented) An architecture that facilitates a reference voltage in a multi-bit memory, comprising:

a multi-bit memory core including a plurality of data cells for storing data;

first and second reference arrays of a plurality of multi-bit reference cells , the first and second reference arrays fabricated on the memory core; and

a first bit value of a first reference cell of the first reference array averaged with a second bit value of a second reference cell of the second reference array to arrive at the reference voltage employed during a data cell read operation.

2. (Original) The architecture of claim 1, the core further comprising a sector of multi-bit data cells organized in rows and columns with associated wordlines (WLn) attached to the multi-bit data cells in a row and with associated bitlines (BLn) attached to the multi-bit data cells in a column, the first and second reference cells forming a multi-bit reference pair that is programmed and erased with the multi-bit data cells during programming and erase cycles.

3. (Original) The architecture of claim 2, the multi-bit reference pair is associated with a word in a wordline (WL0), the multi-bit reference pair utilized during reading of bits of the word.

4. (Original) The architecture of claim 2, the multi-bit reference pair is associated with multi-bit data cells in a wordline (WL0), the multi-bit reference pair utilized during reading of bits in the wordline (WL0).

5. (Original) The architecture of claim 2, further comprising a plurality of the multi-bit reference pairs associated with and attached to a corresponding wordline (WL0), the associated multi-bit reference pair utilized during reading of bits in the corresponding wordline (WL0).

6. (Original) The architecture of claim 2, the multi-bit reference pair is associated with multi-bit data cells in the sector, the multi-bit reference pair utilized during reading of bits in the sector.

7. (Original) The architecture of claim 1, the memory core including a plurality of data sectors that are accessible by the first and second reference arrays, the first and second reference arrays located centrally of the plurality of data sectors.

8. (Original) An integrated circuit comprising the memory of claim 1.

9. (Original) A computer comprising the memory of claim 1.

10. (Original) An electronic device comprising the memory of claim 1.

11. (Original) The architecture of claim 1, the first and second reference arrays including corresponding reference cells that are interweaved among the data cells.

12. (Original) The architecture of claim 1, the memory core further comprising a plurality of data sectors, such that each data sector is associated with at least one of the first reference array and the second reference array of multi-bit reference cells.

13. (Previously Presented) An architecture that facilitates a reference voltage in a multi-bit memory, comprising:

a multi-bit memory core for storing data, the memory core including two groups of data sectors;

first and second reference arrays of a plurality of multi-bit reference cells , the first and second reference arrays fabricated on the memory core interstitial to the groups of data sectors; and

a first bit value of a first reference cell of the first reference array and a second bit value of a second reference cell of the second reference array forming a reference pair whose respective bit values are averaged to arrive at the reference voltage for a read operation.

14. (Original) The architecture of claim 13, the groups of data sectors read in an interleaved manner with a selected reference pair.

15. (Original) The architecture of claim 13, the first and second reference arrays precharged before being averaged.

16. (Original) The architecture of claim 13, further comprising a redundancy array located at least one of proximate and adjacent to the groups of data sectors.

17. (Previously Presented) A method for providing a reference voltage in a multi-bit memory, comprising:

receiving a multi-bit memory core for storing data;

providing first and second reference arrays of a plurality of multi-bit reference cells, the first and second reference arrays fabricated on the memory core; and

averaging a first bit value of a first reference cell of the first reference array with a second bit value of a second reference cell of the second reference array to arrive at the reference voltage utilized during a read operation.

18. (Original) The method of claim 17, the core further comprising a sector of multi-bit data cells organized in rows and columns with associated wordlines (WLn) attached to the multi-bit data cells in a row and with associated bitlines (BLn) attached to the multi-bit data cells in a column, the first and second reference cells forming a multi-bit reference pair that is programmed and erased with the multi-bit data cells during programming and erase cycles.

19. (Original) The method of claim 18, the multi-bit reference pair is associated with a word in a wordline (WL0), the multi-bit reference pair utilized during reading of bits in the word.

20. (Original) The method of claim 18, the multi-bit reference pair is associated with multi-bit data cells in a wordline (WL0), the multi-bit reference pair utilized during reading of bits in the wordline (WL0).

21. (Original) The method of claim 18, further comprising a plurality of the multi-bit reference pairs associated with and attached to a corresponding wordline (WL0), the associated multi-bit reference pair utilized during reading of bits in the corresponding wordline (WL0).

22. (Original) The method of claim 18, the multi-bit reference pair is associated with multi-bit data cells in the sector, the multi-bit reference pair utilized during reading of bits in the sector.

23. (Original) The method of claim 17, the memory core including a plurality of data sectors that are accessible by the first and second reference arrays, the first and second reference arrays located centrally of the plurality of data sectors.

24. (Previously Presented) A system for providing a reference voltage in a multi-bit memory, comprising:

means for providing a multi-bit memory core for storing data;

means for providing first and second reference arrays of a plurality of multi-bit reference cells, the first and second reference arrays fabricated on the memory core ; and

means for averaging a first bit value of a first reference cell of the first reference array with a second bit value of a second reference cell of the second reference array to arrive at the reference voltage to facilitate a read operation.

25. (Previously presented) The system of claim 24, the first and second reference arrays including corresponding reference cells that are interweaved among the data cells.

26. (Previously presented) The system of claim 24, the memory core further comprising a plurality of data sectors, such that each data sector is associated with at least one of the first reference array and the second reference array of multi-bit reference cells.

27. (Previously presented) The system of claim 24, further comprising a redundancy array located at least one of proximate and adjacent to the groups of data sectors.

IX. Evidence Appendix (37 C.F.R. §41.37(c)(1)(ix))

None.

X. Related Proceedings Appendix (37 C.F.R. §41.37(c)(1)(x))

None.